



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/586,909

01/08/2007

Noritaka Muraki

Q79714

1815

23373 7590 06/22/2009
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER

HUBER, ROBERT T

ART UNIT

PAPER NUMBER

2892

MAIL DATE

DELIVERY MODE

06/22/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/586,909	Applicant(s) MURAKI ET AL.	
	Examiner ROBERT HUBER	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 March 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5-17 and 19-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,5-17 and 19-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 May 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. The Examiner acknowledges the amendment(s) to claims 21 and 22 filed on March 27, 2009. The objection(s) to claims 21 and 22 cited in the previous office action filed on November 28, 2008 is (are) hereby withdrawn.
2. Claims 1, 5 – 17, and 19 – 22 objected to because of the following informalities:
 - a. Claim 1 recites "*the multiple quantum well structure*" in line 13 of the claim. This limitation lacks proper antecedent basis. Line 4 of the claim recites "*a quantum well structure*". Therefore, "*the multiple quantum well structure*" is interpreted as "*the quantum well structure*".
 - b. Claim 1 recites "*the well layer*" in the second to last line of the claim (e.g. as seen on page 3 of the claims submitted on March 27, 2009). This limitation lacks proper antecedent basis, and is interpreted as "*the gallium nitride compound semiconductor well layer*".
 - c. Claim 1 recites "*absent a well layer*" in the last line of the claim. It is unclear if the "*a well layer*" is the same well layer as the gallium nitride compound semiconductor well layer as recited in lines 5 - 6 of the claim, or a new, distinct well layer. A best-deemed interpretation is made, and "*absent a well layer*" is interpreted as "*absent the gallium nitride compound semiconductor well layer*".

- d. Claims 5 – 17 and 19 – 22 depend from claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The Examiner acknowledges the amendment(s) to claim 1 filed on March 27, 2009. The rejection of claims 1, 5 - 17, and 19 - 22 under USC 112, second paragraph, cited in the previous office action filed on November 28, 2008 is (are) hereby withdrawn.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 5 - 17, and 19 - 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "*the individual well layers*" of the quantum well structure in line 13. There is insufficient antecedent basis for this limitation in the claim. Lines 5 – 6 recite "*a gallium nitride compound semiconductor well layer...*" as part of the quantum well structure. A best-deemed interpretation is made, and "*the individual well layers*" is interpreted as "*the gallium nitride compound semiconductor well layer*".

Claims 5 – 17 and 19 – 22 depend from claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 5, 9 – 11, 16, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 6,608,330 B1, prior art of record) in view of Sasaoka (US 2003/0042496 A1, prior art of record).

a. Regarding claim 1, **Yamada discloses a gallium nitride compound semiconductor light-emitting device** (e.g. figure 1) **comprising**
a crystalline substrate (substrate 101);
a light-emitting layer of a quantum well structure (active layer 106)
that is formed of a gallium nitride compound semiconductor barrier layer

Art Unit: 2892

doped with an impurity element (layers 107, disclosed in col. 11, lines 7 – 8 to be formed of GaN, InGaN, AlGaN, or the like. E.g. AlGaN may be considered to be doped GaN with impurity element Al) **and a gallium nitride compound semiconductor well layer undoped with any impurity element** (layers 108, disclosed in col. 10, lines 3 – 4 to be undoped), **said light-emitting layer being provided on a second side of the crystalline substrate** (e.g. as seen in figure 1);

a contact layer formed of a Group III-V compound semiconductor for providing an Ohmic electrode for supplying device operation current to the light-emitting layer (layer 111, formed from GaN as stated in col. 8, line 41);
and

an Ohmic electrode (electrode 112)) **that is provided on the contact layer** (e.g. as seen in figure 1) **and has an aperture through which a portion of the contact layer is exposed** (e.g. as seen in figure 1, the sides of electrode 112 are open, exposing the contact layer 111),

wherein the Ohmic electrode exhibits light permeability with respect to light emitted from the light-emitting layer (col. 10, line 42 discloses the electrode 112 to be transparent), **the gallium nitride compound semiconductor well layer of the quantum well structure** each has the same **composition** (e.g. as seen in figure 1, there are multiple gallium nitride compound semiconductor well layers 108. Since the multiple well layers are all designated as a well layer 108, it is anticipated they are all of the same structure

Art Unit: 2892

and all have the same composition) **and contains a thick portion having a large thickness and a thin portion having a small thickness** (e.g. col. 13, lines 16 - 36, with reference to figure 6, disclose that the well layers have both thin and thick regions), **and a portion having a thickness of 0 nm to 1.5 nm** (col. 13, lines 20 – 22 disclose that, with reference to figure 6, disclose that the well layers have regions with thickness less than half of the average thickness. Col. 9, lines 35 - 36 discloses the average thickness of a well layer to be 3 nm. Therefore, the regions defined by "D" in figure 6 of the well layers are less than 1.5 nm);

wherein the gallium nitride compound semiconductor well layer is a discontinuous layer (A common definition of "discontinuous" is "marked by breaks or interruptions". col. 13, lines 20 – 22 disclose that, with reference to figure 6, the well layer may be considered as having "breaks" or "interruptions" in regions with lower thicknesses than other regions, and there for the well layer may be considered as "discontinuous") **and the light-emitting layer has a region absent the gallium nitride compound semiconductor well layer** (e.g. light emitting layer 106 has a region comprising layer 107 which is absent the gallium nitride compound semiconductor well layer 108).

Yamada is silent with respect to disclosing the barrier layer is doped with a Group IV element at an average atom density of $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$.

Sasaoka discloses a gallium nitride compound semiconductor light-emitting device with barrier layer being doped with a Group IV element at an average atom density of $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$ which exhibits a low resistance (¶ [0109] discloses the barrier layer to be Si doped with a concentration of $1 \times 10^{18} \text{ cm}^{-3}$).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Yamada such that the barrier layers are doped with a Group IV compound with a density of $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$ since it was known that gallium nitride compound light emitting devices can contain quantum well layers comprising barrier layers with such dopant and concentrations, as disclosed by Sasaoka. One would have been motivated to make the barrier layer with a dopant of Group IV materials since these would create an n-type semiconductor barrier layer, allowing one to control the conductivity of the barrier layer, resulting in a more efficient light emission properties of the quantum well.

Regarding the limitation of doping the barrier layer “*for the purpose of decreasing forward voltage of the device*”, this is regarded as a statement of intended use, and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114.

b. Regarding claim 5, **Yamada in view of Sasaoka further disclose a gallium nitride compound semiconductor light-emitting device, as cited above, wherein the predetermined impurity element added only to the barrier layer is silicon** (Yamada: col. 10, lines 3 – 7, disclose that the layer 108 may be doped with Silicon. Col. 9, line 62 discloses the layer 108 may be a barrier layer).

c. Regarding claim 9, **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada is silent with respect to the contact layer having a thickness of 1 μm to 3 μm , however Yamada discloses that the contact layer thickness is 0.25 μm .**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enlarge the layer thickness of Yamada in view of Sasaoka, since it has been held by the courts that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device, and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225

Art Unit: 2892

USPQ 232 (1984). One would be motivated to make such a modification of the layer thickness in order to make the device structurally more rigid.

d. Regarding claim 10, **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the Ohmic electrode (18) exhibits a transmittance at the wavelength of emitted light of 30% or higher** (the structure of Yamada in view of Sasaoka are obvious over the structure of the claimed invention, therefore Yamada in view of Sasaoka are obvious over the properties of the light transmittance of the Ohmic electrode, since it has been held that when the prior art discloses the structure of the claimed invention, a prima facie case of anticipation or obviousness of the inherent properties has been established. See MPEP 2112.01.)

e. Regarding claim 11, **Yamada in view of Sasaoka further disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the Ohmic electrode has a thickness of 1 nm to 100 nm** (Yamada: col. 10, lines 42 – 43, disclose the electrode has a thickness of 20 nm).

f. Regarding claims 16 and 17, **Yamada in view of Sasaoka further disclose a lamp and an LED employing the gallium nitride compound**

Art Unit: 2892

semiconductor light- emitting device according to claim 1 (Yamada: col. 11, lines 25 – 36).

g. Regarding claim 19, **Yamada in view of Sasaoka further disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the barrier layer is an Si-doped n-type GaN barrier layer** (Sasaoka: ¶ [0109] discloses the Group IV doped GaN barrier layer to be Si doped n-type GaN).

9. Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view Sasaoka, and in further view of Hanaoka et al. (US 5,804,839, prior art of record).

a. Regarding claim 6, **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above. However, Yamada and Sasaoka are silent with respect to the contact layer being doped with an n- type impurity element and has a carrier concentration of $5 \times 10^{18} \text{ cm}^{-3}$ to $2 \times 10^{19} \text{ cm}^{-3}$.**

Hanaoka teaches that GaN layers may be formed with n-type impurity concentrations of $1 \times 10^{19} \text{ cm}^{-3}$ (col. 9, lines 20 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the contact layer of Yamada in view Sasaoka to include n-type impurities with a concentration of $1 \times 10^{19} \text{ cm}^{-3}$ since Hanaoka

Art Unit: 2892

discloses that this is known structure used for light emitting devices. One would have been motivated to make such a modification since it would allow the layer to exhibit light transmission properties, allowing the light to transmit readily through the layer, and desirable electrical properties for tuning the light emitting device.

b. Regarding claims 7 and 8, **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the contact layer is doped with a p - type impurity element** (Yamada: col. 8, line 41). **Yamada and Sasaoka are silent with respect to the layer having a carrier concentration of $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$.**

Hanaoka teaches that p-type contact layers may be doped with a carrier concentration of $1 \times 10^{18} \text{ cm}^{-3}$ (col. 3, lines 48 – 49).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the contact layer of Yamada in view of Sasaoka to have a p-type impurity concentration of $1 \times 10^{18} \text{ cm}^{-3}$ since Hanaoka discloses that this is known contact layer structure used in light emitting devices. One would have been motivated to make such a modification since it would allow the layer to exhibit light transmission properties, allowing the light to transmit readily through the layer, and desirable electrical properties for tuning the light emitting device.

10. Claims 12, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Sasaoka, and in further view of Morita et al. (US 6,121,636, prior art of record). **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada and Sasaoka are silent with respect to a multilayered metallic reflecting mirror made of the same material identical to the Ohmic electrode for reflecting light emitted from the light-emitting layer to the outside, which is provided on a first side of the crystalline substrate.**

Morita discloses a mirror on the outside first side of the crystalline substrate (e.g. figure 1, reflecting layer 11) **wherein the metallic reflecting mirror contains a metallic material identical to that contained in the Ohmic electrode** (e.g. col. 4, lines 1 – 9, discloses that the layer may be made of gold, which is the same material as the electrode 9). **Morita further discloses that the layers may be multilayered** (col. 2, lines 21 - 25).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Yamada in view of Sasaoka to include the reflecting mirror, as taught by Morita, since Morita discloses that multilayer reflecting mirrors, made of the same material as the electrode, can be added to light emitting devices. One would be motivated to add a reflecting mirror on the second side of the substrate in order to prevent light escaping from the bottom of the device, thereby protecting underlying structures, as taught in Morita in col. 8, lines 33 - 44. One would

Art Unit: 2892

be motivated to make the reflecting mirror multilayered to enhance its reflecting ability.

One would further be motivated to make the mirror of the same material as that of the Ohmic electrode since it would require fewer materials for the production process.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Sasaoka, and in further view of Kaneyama et al. (US 6,452,214 B2, prior art of record). **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada and Sasaoka are silent with respect to a metallic reflecting mirror containing a single-metal film or an alloy film formed from at least one member selected from the group consisting of silver, platinum, rhodium and aluminum.**

Kaneyama teaches a metallic reflecting mirror formed from aluminum (col. 4, lines 32 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Yamada in view of Sasaoka to include the reflecting mirror, as taught by Kaneyama, since Kaneyama discloses that reflecting mirrors made of aluminum can be added to light emitting devices. One would be motivated to add an aluminum reflecting mirror on the second side of the substrate in order to prevent light escaping from the bottom of the device, thereby protecting underlying structures, and aluminum is a readily available material that is can be

Art Unit: 2892

relatively easily deposited on substrates via known deposition methods (i.e. sputtering, evaporation, etc...)

12. Claims 20 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Sasaoka as applied to claim 1 above, and further in view of Lester (US 6,291,839 B1, prior art of record).

a. Regarding claim 20, **Yamada in view of Sasaoka disclose a gallium nitride compound semiconductor light-emitting device according to claim 1, but are silent with respect to apertures are formed such that a total surface area of the apertures accounts for 30% to 80% of a surface of the contact layer.**

Lester discloses a gallium nitride compound semiconductor light-emitting device (e.g. figure 1), wherein apertures are formed in an Ohmic electrode (openings in p-type contact 20, as disclosed in col. 3, lines 1 - 3) such that a total surface area of the apertures accounts for 30% to 80% of a surface of the contact layer (as disclosed in col. 4, lines 34 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the gallium nitride semiconductor light-emitting device of Yamada in view of Sasaoka such that the Ohmic electrode comprises a apertures with a total surface area of 30 - 80% of the surface of contact layer since Lester discloses a similar device with similar structure wherein apertures with such configurations may be formed. One would have been motivated to

have apertures of such dimensions in order to optimize light transmittance from the device while providing an even Ohmic contact, as discussed by Lester (col. 3, lines 34 - 40).

b. Regarding claim 21, **Yamada in view of Sasaoka disclose gallium nitride compound semiconductor light-emitting device according to claim 1, wherein a metallic film consists the Ohmic electrode** (Yamada: col. 10, lines 42 – 43 disclose electrode 112 to be gold and nickel). **Yamada in view of Sasaoka are silent with respect to a minimum horizontal width (lateral width) of the metallic film consisting the Ohmic electrode is 10 μm or less, and a horizontal width of the aperture is 0.5 μm to 50 μm .**

Lester discloses a gallium nitride compound semiconductor light-emitting device (e.g. figure 1), **wherein a horizontal width of the aperture is 0.5 μm to 50 μm** (e.g. figure 1 and col. 3, lines 1 -3 disclose that the Ohmic layer may comprise openings (apertures). Col. 3, lines 21 – 22 disclose the dimensions of the openings). **Lester also discloses that a total surface area of the apertures accounts for 30% to 80% of a surface of the contact layer** (as disclosed in col. 4, lines 34 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Yamada in view of Sasaoka such that the Ohmic electrode comprises apertures with a horizontal width of 0.5 μm to 50 μm since Lester discloses a similar device with an Ohmic layer comprising

apertures of such dimensions. One would have been motivated to have the apertures of a width between $0.5\text{ }\mu\text{m}$ to $50\text{ }\mu\text{m}$ in order to maximize current flow in the Ohmic contact while optimizing the light transmittance through the apertures of the Ohmic layer, as discussed by Lester (col. 3, lines 5 – 22).

The combination of Yamada in view of Sasaoka with the teachings of Lester disclose a device that is obvious over the limitation of a minimum horizontal width (lateral width) of a metallic film consisting the Ohmic electrode is $10\text{ }\mu\text{m}$ or less. Yamada discloses the device to have an area of $350\text{ }\mu\text{m}$ square (col. 10, line 53), of which the Ohmic layer of Yamada in view of Sasaoka and Lester comprises a large portion (e.g. as seen in figures 1 of Yamada and Lester). Since Lester discloses the total surface area of the apertures to account for 20 - 80% of the surface area, and the dimensions of the apertures to be $0.5 - 20\text{ }\mu\text{m}$, one may do the calculations to find the average horizontal distance between the apertures to be about $0.4\text{ }\mu\text{m}$.

Although this calculation is done using an estimated contact layer size similar to the size of the area of device as disclosed by Yamada, and average homogeneous distribution of apertures within the Ohmic contact layer, a prima facie case of obviousness is established that a minimum horizontal width of the metallic film comprising the Ohmic electrode is $10\text{ }\mu\text{m}$ or less, and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to have a

Art Unit: 2892

minimum horizontal distance of the metallic film comprising the Ohmic electrode of 10 μm or less in order to optimize the current flow in the Ohmic contact while optimizing the light transmittance through the apertures of the Ohmic layer, as discussed by Lester (col. 3, lines 5 – 22).

c. Regarding claim 22, **Yamada in view of Sasaoka and in further view of Lester disclose a gallium nitride compound semiconductor light-emitting device according to claim 20, wherein a horizontal width of the aperture is 0.5 mm to 50 mm (Lester: col. 3, line 22).**

Regarding the claim limitation “wherein a minimum horizontal width (lateral width) of a metallic film consisting the Ohmic electrode is 10 mm or less”, the combination of Yamada in view of Sasaoka with the teachings of Lester disclose a device that is obvious over the limitation of a minimum horizontal width (lateral width) of a metallic film comprising the Ohmic electrode is 10 μm or less. Yamada discloses the device to have an area of 350 μm square (col. 10, line 53), of which the Ohmic layer of Yamada in view of Sasaoka and Lester comprises a large portion (e.g. as seen in figures 1 of Yamada and Lester). Since Lester discloses the total surface area of the apertures to account for 20 - 80% of the surface area, and the dimensions of the apertures to be 0.5 – 20 μm , one may do the calculations to find the average horizontal distance between the apertures to be about 0.4 μm .

Although this calculation is done using an estimated contact layer size similar to the size of the area of device as disclosed by Yamada, and average homogeneous distribution of apertures within the Ohmic contact layer, a prima facie case of obviousness is established that a minimum horizontal width of the metallic film comprising the Ohmic electrode is 10 μm or less, and it has been held that when the prior art discloses the general conditions of the claimed invention, discovering the optimum or workable ranges involves only ordinary skill in the art. See MPEP 2144.05. One would have been motivated to have a minimum horizontal distance of the metallic film comprising the Ohmic electrode of 10 μm or less in order to optimize the current flow in the Ohmic contact while optimizing the light transmittance through the apertures of the Ohmic layer, as discussed by Lester (col. 3, lines 5 – 22).

Response to Arguments

13. Applicant's arguments with respect to claim 1 filed on March 27, 2009 have been fully considered but they are not persuasive. At present, the prior art of Yamada in view of Sasaoka remains commensurate to the scope of the claim as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above.

a. In response to Applicants arguments drawn to the amendment "the gallium nitride compound semiconductor well layer of the quantum well structure each has the same composition", the prior art of Yamada discloses such a

limitation. As cited above with respect to claim 1, Yamada discloses in figure 1 several layers that form the gallium nitride compound semiconductor well layer 108. Since all of the layers are designated with the same number “**108**” in figure 1, it is anticipated that all of the layers have the same composition. The Applicant has argued that Yamada discloses that well layers **108** and **109** have a different composition, however this argument is moot in light of the Examiner's interpretation of the well layer to only comprise well layers **108**, and not **109**.

b. In response to Applicants arguments drawn to the amendment “the gallium nitride compound semiconductor well layer is a discontinuous layer and the light-emitting layer has a region absent a gallium nitride compound semiconductor well layer”, the prior art of Yamada discloses such limitations. As cited above with respect to claim 1, a common definition of “discontinuous” is “marked by breaks or interruptions”. Yamada discloses in col. 13, lines 20 – 22 that, with reference to figure 6, the well layer may be considered as having “breaks” or “interruptions” in regions where the thickness of the well layer changes abruptly at regions of a lower thicknesses than other regions. This abrupt change in thickness may be considered a “break” or “interruption” in the well thickness, and therefore for the well layer may be considered as “discontinuous.”

Yamada also discloses a region of the light emitting layer 106 that is absent a gallium nitride compound semiconductor well layer 108. As clarified in

figure 1, the region of the light emitting layer 106 comprising the barrier layers 107 may be considered as a region that is absent the gallium nitride compound semiconductor well layer 108.

c. With respect to the Applicant's arguments that Yamada does not disclose the gallium nitride compound semiconductor well layer of the quantum well structure each have a thick portion having a large thickness and a thin portion having a small thickness and a portion having a thickness of 0 nm to 1.5 nm (as presented on pages 9 – 10 of the Remarks), the Examiner respectfully disagrees. The Applicant argues that Yamada teaches away from the invention by stating Yamada discloses "*that when the well layer has smoother growth surfaces with barrier layer and better crystallinity, it's luminous efficiency is improved. Column 4, lines 16 - 35*" (page 9 of Remarks). However, in column 4, lines 21 – 23 Yamada remarks that "*it is not always true*" that smoother growth surfaces yield an improved efficiency. In col. 4, lines 31 - 35 Yamada discusses the improved efficiency with an optimized surface roughness (asperity) of the second well layer. Furthermore, Yamada discloses, as cited above with respect to claim 1, the well layer to have a certain surface roughness, as seen in figure 6. For example, col. 13, lines 20 – 22 disclose that the well layers have regions with thickness less than half of the average thickness. Col. 9, lines 35 - 36 discloses the average thickness of a well layer to be 3 nm. Therefore, the regions defined by "D" in figure 6 of the well layers are less than 1.5 nm. Therefore, Yamada

Art Unit: 2892

discloses a claimed limitation, and the argument that Yamada teaches away from the claimed invention is not found persuasive.

d. With respect to the Applicant's arguments that Yamada does not disclose "*a gallium nitride compound semiconductor barrier layer doped with an impurity element*", the Examiner respectfully disagrees. The Applicant argues that the Examiner's interpretation of AlGa_N to be doped Ga_N not valid, and that AlGa_N may not be considered Ga_N doped with an impurity of element of Al. The Applicant argues that that expression "*doping a semiconductor with an impurity*" implies controlling the band structure, such as an energy gap, and the adjusting the concentration of electrons and holes. The Applicant argues that since the addition of Al does not change the electron/hole concentration, it may not be considered an "impurity" element added to Ga_N. The Examiner reminds that Applicant that claims must be given their broadest reasonable interpretation, as per MPEP 2111. It is maintained by the Examiner that one may consider Al to be an impurity element of a compound of Ga_N since one may add Al to Ga_N to obtain AlGa_N. A common definition of "impurity" is "that which renders anything impure". One may indeed consider the addition of Al to Ga_N to render the material Ga_N as "impure". The claimed limitation of "*an impurity element*" does NOT imply any band structure change or electron/hole concentration difference, but rather it simply implies the addition of an element relative to an different material (e.g. combination of Al with Ga_N) Therefore, with the claims given their

Art Unit: 2892

broadest reasonable interpretation, it is maintained by the examiner that AlGaIn may be considered GaIn with an added impurity element of Al.

e. With respect to the Applicant's arguments that Sasaoka does not disclose or teach a range of average atom concentration of the group IV element doped in to the barrier layer for lowering the forward voltage without varying emission wavelength (as presented on pages 11 - 12 of the Remarks), the Examiner respectfully disagrees. The Examiner notes that the rejection of claim 1 is over Yamada in view of Sasaoka, wherein it is Sasaoka is used a secondary reference to teach the barrier layer being doped with a Group IV element with an average atomic density of $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$. Yamada discloses a barrier layer (107), but fails to teach it being doped with a Group IV element. Yamada does disclose the barrier layer to be made of materials such as GaIn, InGaIn, AlGaIn, and the like (Col. 11, lines 7 - 8). Sasaoka discloses a similar light emitting device as Yamada, including a light emitting layer comprising a quantum well structure with alternating well layers and barrier layers, wherein the barrier layer is made of InGaIn and is doped with silicon with a concentration of $1 \times 10^{18} \text{ cm}^{-3}$ ([0109] of Sasaoka). Silicon is a Group IV element, which is doped into the InGaIn barrier layer yielding a concentration within the claimed range (See MPEP 2131.03). Therefore, the combination of Yamada in view of Sasaoka renders obvious the claim limitation. The limitation of doping the barrier layer "*for the purpose of decreasing the forward voltage of the device*" is considered a

statement of intended use, and it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114. The combination of Yamada in view of Sasaoka renders obvious the claimed structure, and therefore renders obvious the claimed invention.

14. Applicant's arguments with respect to claims 21 and 22 filed on March 27, 2009 have been fully considered but they are not persuasive. The Applicant's argues that the prior art of Lester does not disclose "*a horizontal width of the aperture is 0.5 μ m to 50 μ m*". The Examiner respectfully disagrees. The Applicant argues that Lester discloses in col. 3, lines 17 - 30 that the opening of the p-type contact 20 in excess of 4 μ m will produce a "spotty" emission pattern (pages 12 - 13 of Remarks). It is acknowledged that Lester states that there is a preferred maximum for the opening, which is disclosed to be 2 μ m (col. 3, line 22). This preferred maximum opening is within the claimed range of the aperture width of 0.5 μ m to 50 μ m, and therefore Lester discloses the claimed limitation (See MPEP 2131.03). The combination of the teachings of the aperture width of Lester with the device of Yamada in view of Sasaoka renders obvious the claimed invention as recited in claims 21 and 22.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2892

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
June 12, 2009